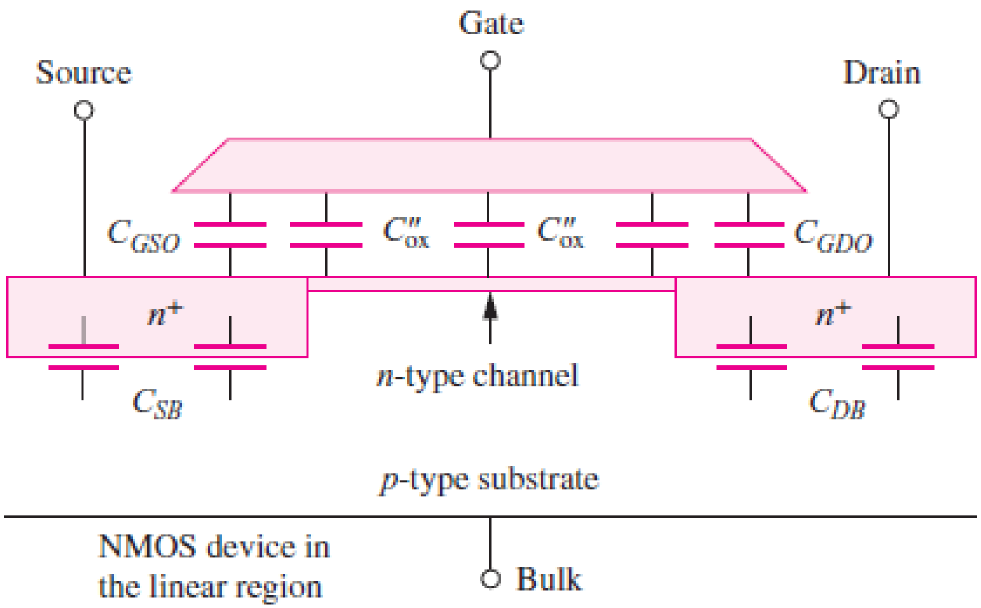
Announcements

- No office hours today or Thursday (catching a plane right after class).
- Emily Allstot (TA) will give Friday lecture.
- Exam 2 in class on Monday 5/19
  - MOSFETs
  - MOSFETs in circuits and NMOS Logic
  - HWs 4-6

MOSFET Capacitances: Linear



Gate to Channel capacitance in inversion (or accumulation) :

$$C_{GC} = WLC_{ox}''$$

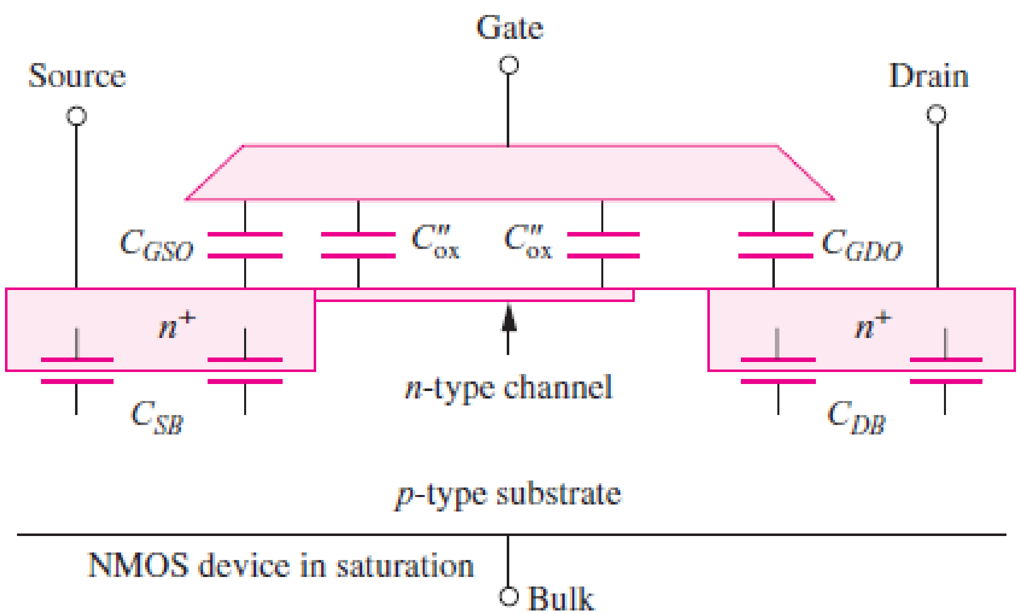
This is split between S and D:

$$C_{GS} = WLC_{ox}''/2 + WCGS_0$$
$$C_{GD} = WLC_{ox}''/2 + WCGD_0$$

There is also capacitance to body (diode area and sidewall)

$$C_{SB} = A_S C_j'' + P_S C_{jSW}'$$
$$C_{DB} = A_D C_j'' + PDCjSW'$$

MOSFET Capacitances: Saturation



In saturation, This is split between S and D:

$$C_{GS} = (2/3)WLC_{ox}'' + WCGS_0$$

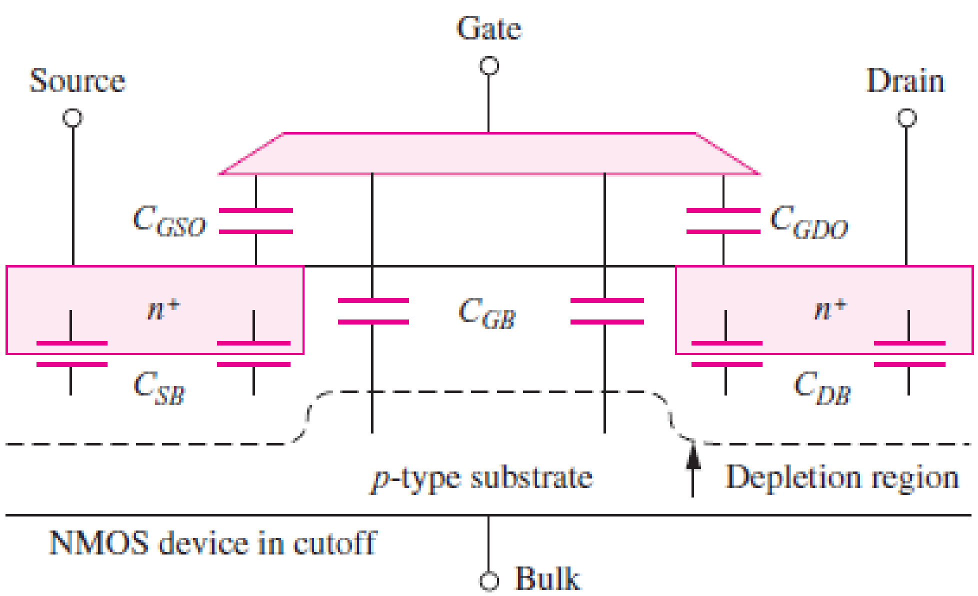
$$C_{GD} = WCGD_0$$

Still capacitance to body (diode area and sidewall)

$$C_{SB} = A_S C_j'' + P_S C_{jSW}'$$

$$C_{DB} = A_D C_j'' + PDCjSW'$$

MOSFET Capacitances: Cutoff



In cutoff, just overlap capacitance remains between G and S/D:

$$C_{GS} = WC_{GS0}$$
$$C_{GD} = WCGD_0$$

Small capacitance between gate and body

$$C_{GB} = LC_{GB0}$$

MOSFET Spice Model

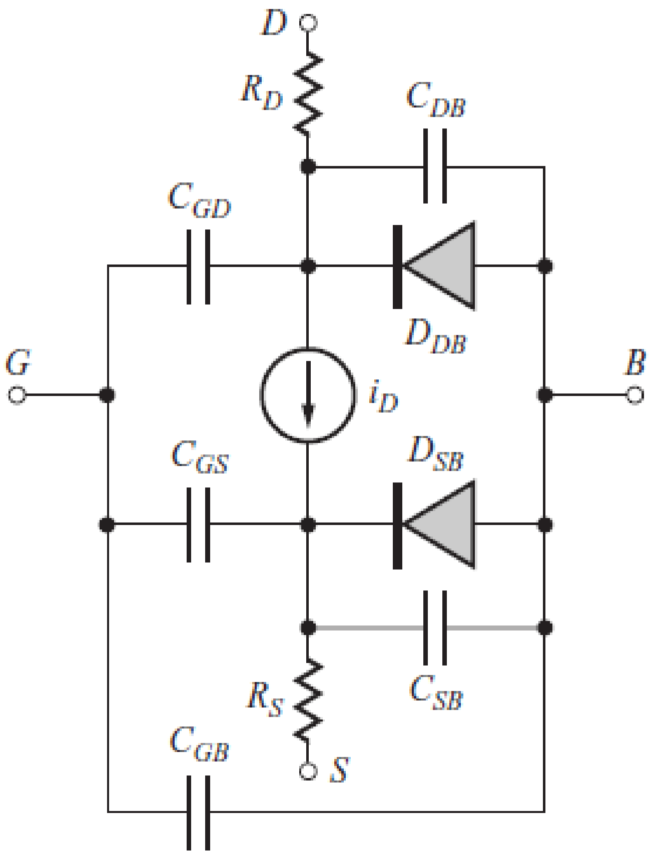


TABLE 4.2
SPICE Parameter Equivalences

PARAMETER	OUR TEXT	SPICE	DEFAULT
Transconductance	K'_n or K'_p	KP	20 µA/V^2
Threshold voltage	V_{TN} or V_{TP}	VT	—
Zero-bias threshold voltage	V_{TO}	VTO	1V
Surface potential	$2\phi_F$	PHI	0.6 V
Body effect	γ	GAMMA	0
Channel length modulation	λ	LAMBDA	0
Mobility	μ_n or μ_p	UO	600 cm^2/V · s
Gate-drain capacitance per unit width	C_{GDO}	CGDO	0
Gate-source capacitance per unit width	C_{GSO}	CGSO	0
Gate-bulk capacitance per unit length	C_{GBO}	CGBO	0
Junction bottom capacitance per unit area	C_J	CJ	0
Grading coefficient	MJ	MJ	0.5 V$^{0.5}$
Sidewall capacitance	C_{JSW}	CJSW	0
Sidewall grading coefficient	MJSW	MJSW	0.5 V$^{0.5}$
Oxide thickness	T_{ox}	TOX	100 nm
Junction saturation current	I_S	IS	10 fA
Built-in potential	ϕ_j	PB	0.8 V
Ohmic drain resistance	—	RD	0
Ohmic source resistance	—	RS	0

EE 331 Devices and Circuits I

Chapter 6

Digital Electronics

Boolean Algebra

- Each statement is either “False” or “True”
- Assign a value to false (0) and another value to true (1)
- 3 most basic operations: NOT, AND, OR

Boolean Algebra: Truth Tables

NOT

$Z = \bar{A}$

A	Z
0	1
1	0

OR

$Z = A + B$

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

AND

$Z = AB$

A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

NOR

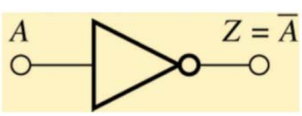
$Z = \overline{A + B}$

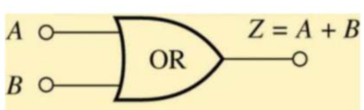
A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

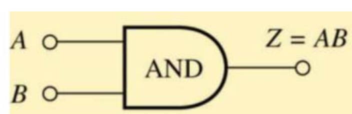
NAND

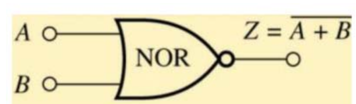
$Z = \overline{AB}$

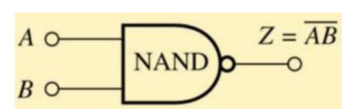
A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0











- True = “1”, False = “0”
- NOR = NOT(OR), NAND = NOT(AND)

Boolean Identities

$A + 0 = A$	$A \cdot 1 = A$	Identity operation
$A + B = B + A$	$AB = BA$	Commutative law
$A + (B + C) = (A + B) + C$	$A(BC) = (AB)C$	Associative law
$A + BC = (A + B)(A + C)$	$A(B + C) = AB + AC$	Distributive law
$A + \overline{A} = 1$	$A \cdot \overline{A} = 0$	Complements
$A + A = A$	$A \cdot A = A$	Idempotency
$A + 1 = 1$	$A \cdot 0 = 0$	Null elements
$\overline{A} + \overline{B} = \overline{AB}$	$\overline{A + B} = \overline{A}\ \overline{B}$	DeMorgan's theorem

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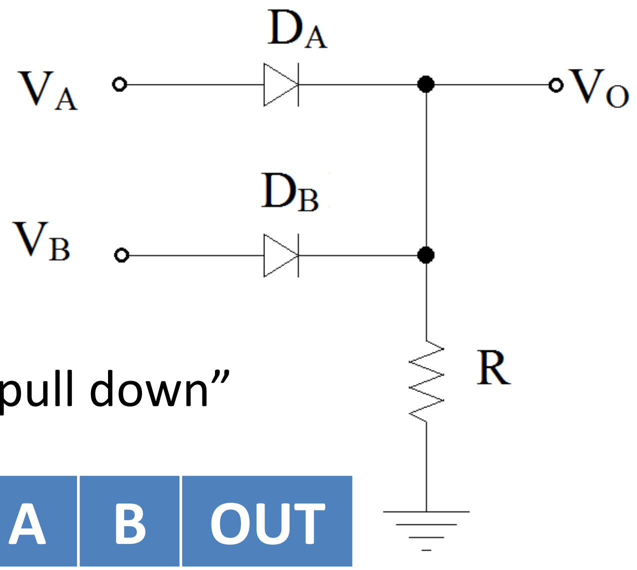
Diode Logic

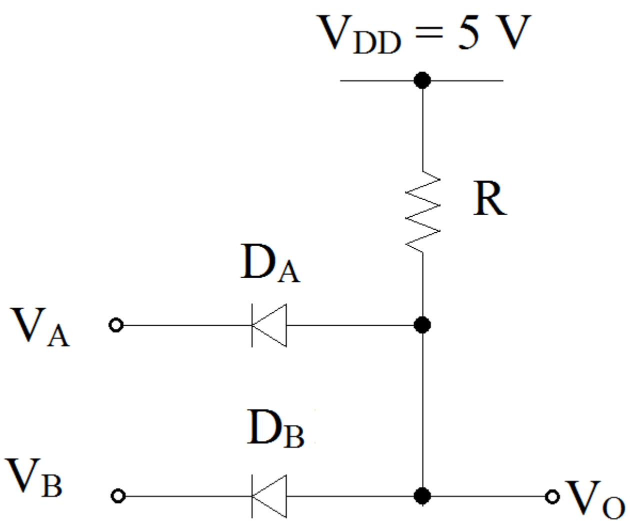


"pull down"

A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	1

- D: $\{V_{on} = 0.7\ V,\ R_{on} = 0\ \Omega\}$
- If V_A and V_B both Low, D_A and D_B both off, $V_O = 0$ V (L)
- If either V_A or V_B (or both) go High (e.g. 5V), then D_A or D_B (or both) turn on, and V_O=5V-V_{on}=4.3V (H)
- OR gate

Diode Logic



"pull-up"

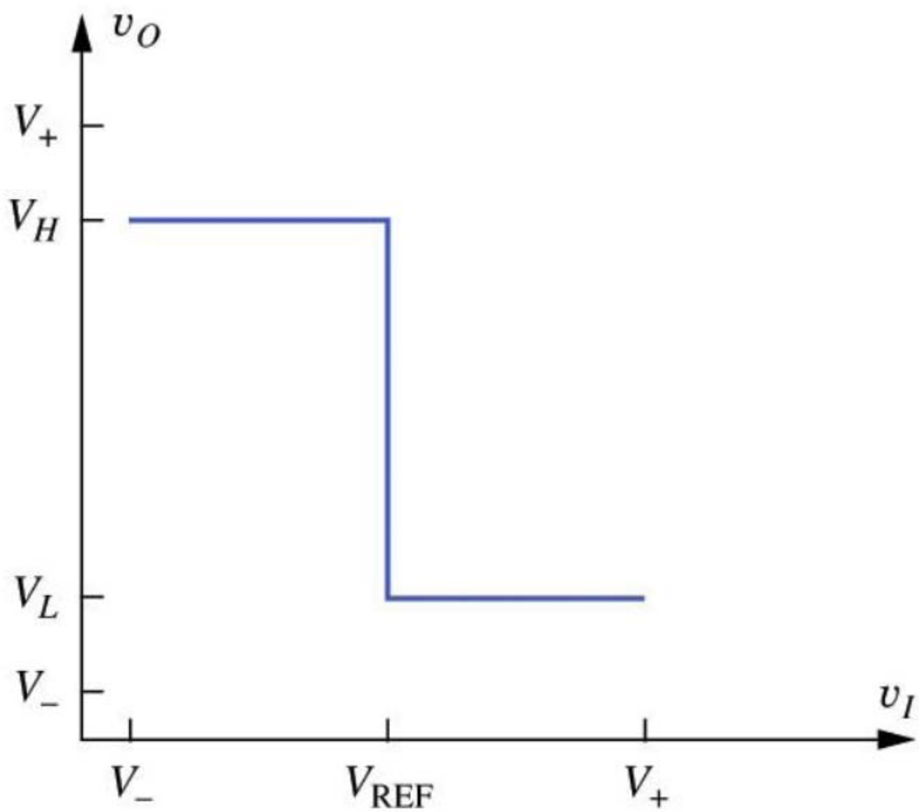
- AND gate

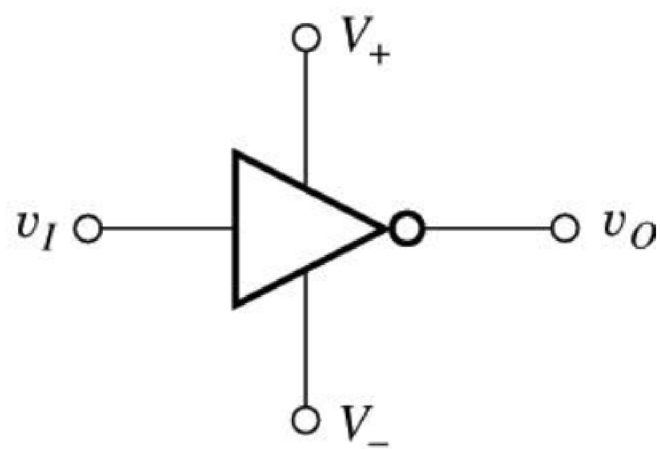
A	B	OUT
0	0	0
0	1	0
1	0	0
1	1	1

Inverter

- Basic building block of digital logics
- NOT operation:
  - Input TRUE (1) => output FALSE (0)
  - Input FALSE (0) => output TRUE (1)
- Inverter
  - input high voltage => output low voltage
  - input low voltage => output high voltage

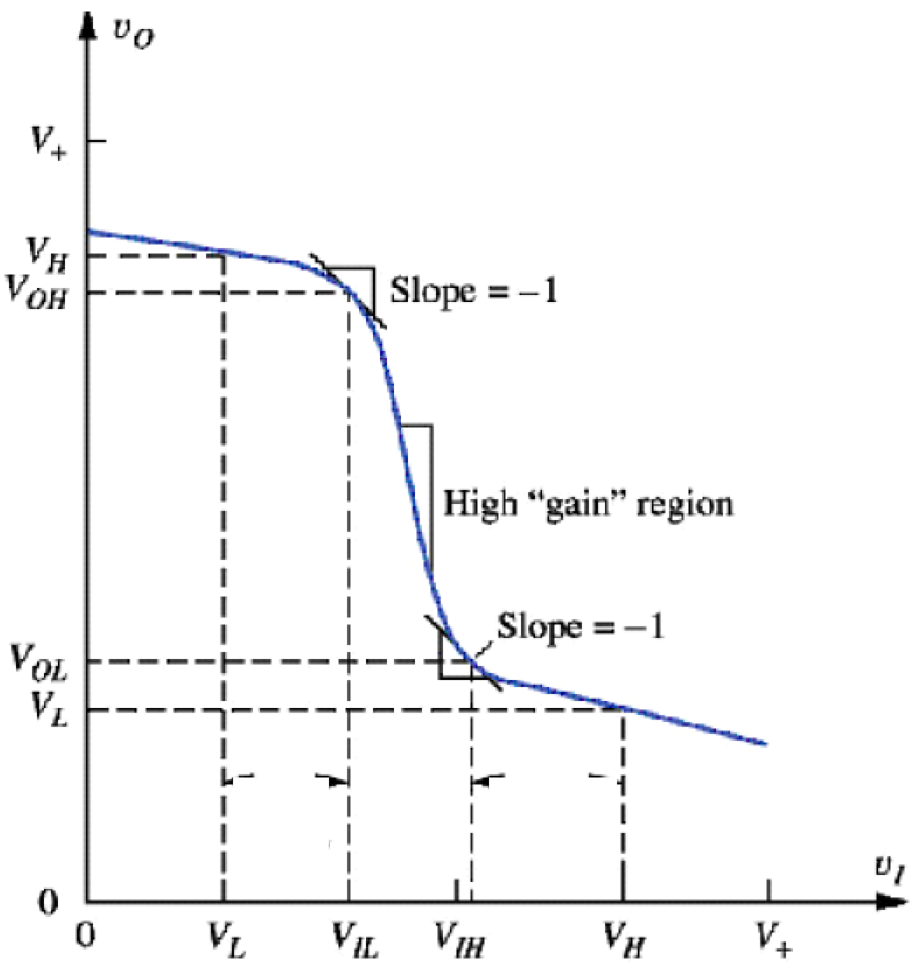
Ideal Inverter





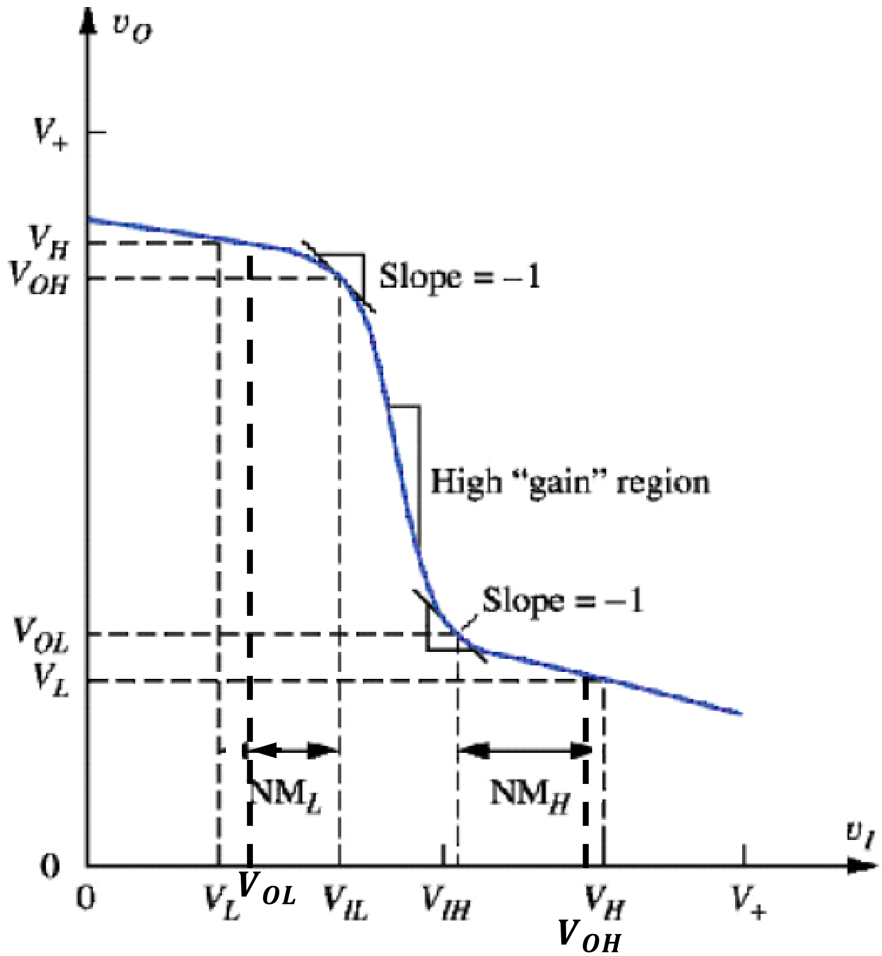
- Requires an extra external power source

"Real" Inverter



- $\boldsymbol{V_{IL}}$: Maximum v_I recognized as a low input logic level.
- $\boldsymbol{V_{IH}}$: Minimum v_I recognized as a high input logic level.
- $\boldsymbol{V_{OH}}$: The v_O corresponding to an input voltage of V_{IL}.
- $\boldsymbol{V_{OL}}$: The v_O corresponding to an input voltage of V_{IH}.
- V_L : Nominal output voltage corresponding to a low-logic state for $v_I = V_H$.
- V_H : Nominal output voltage corresponding to a high-logic state for $v_I = V_L$.

"Real" Inverter

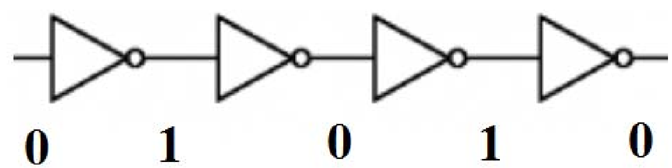


- $(V_{IL}, V_{OH}), (V_{IH}, V_{OL})$: the -1 slope points
- For $0 \leq v_I \leq V_{IL}$ (input low) => $V_{OH} \leq v_O \leq V_+$ (output high)
- For $V_{IH} \leq v_I \leq V_+$ (input high) => $0 \leq v_O \leq V_{OL}$ (output low)
- For $V_{IL} \leq v_I \leq V_{IH}$: undefined logic state

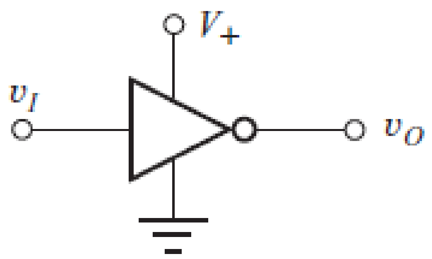
Noise Margin

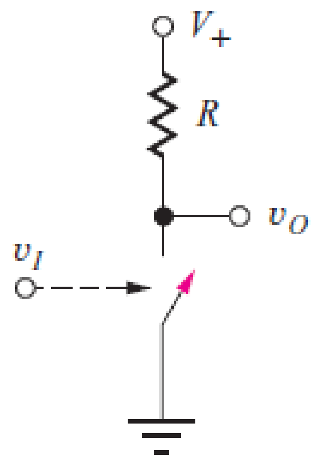
- Noise margins represent “safety margins” that prevent the circuit from producing erroneous outputs in the presence of noisy inputs
- Noise margins are defined for low and high input levels by:

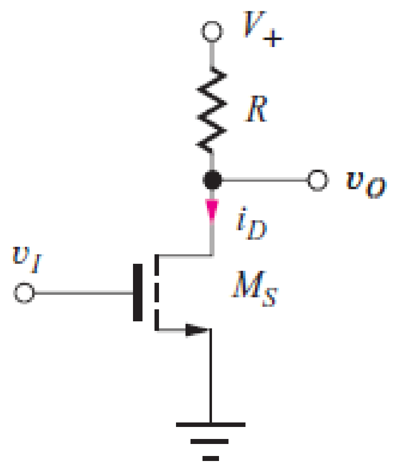
$$NM_L = V_{IL} - V_{OL}$$
$$NM_H = V_{OH} - V_{IH}$$



Sample Inverter Circuits







NMOS Logic Design

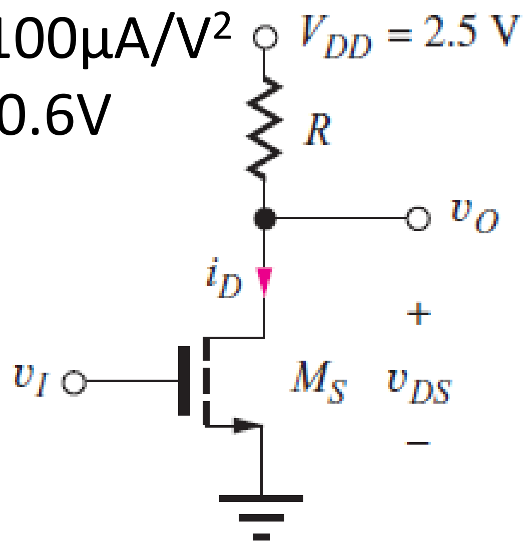
- Designer's job: choose the circuit topology and the *W/L* ratios of the MOS transistors to achieve the desired logic function
- Power supply voltage V_{DD}
  - 1.8–3.3 V power supply levels have gained widespread use. Even lower now.
  - Many portable low-power systems (cell phones) have voltages around 1.0 - 1.5 V

NMOS Logic Design

- Inverters with different NMOS load configurations:
  - the resistor load
  - saturated load
  - depletion-mode load
  - linear load
  - pseudo NMOS

NMOS resistive load inverter

K_n'=100µA/V^2
V_{TN}=0.6V



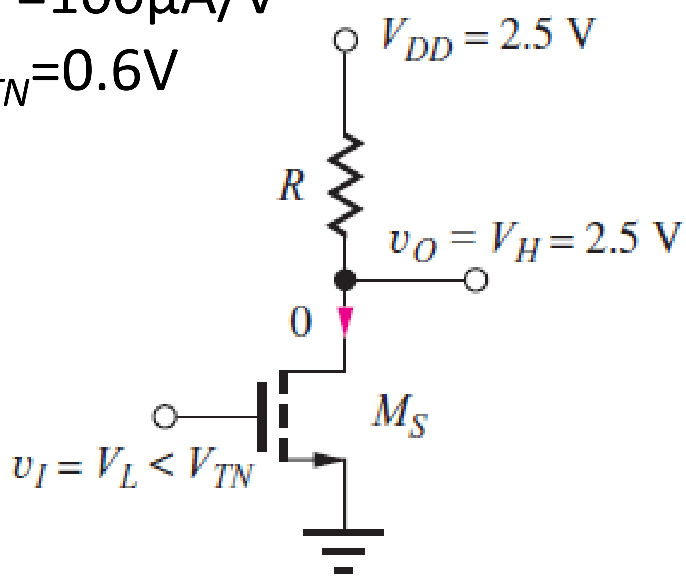
$v_I = v_{GS}, v_O = v_{DS}$

Design: Chose R and W/L of M_S

- A resistor load to "pull" the output up toward the power supply V_{DD}.
- Switch between two states:
  - Triode region: $v_I = V_H \Rightarrow v_O = V_L$
  - Cutoff region: $v_I = V_L \Rightarrow v_O = V_H$

NMOS resistive load inverter

K_n'=100μA/V²
V_{TN}=0.6V



$v_I = V_L, v_O = V_H$

$v_I = V_L$, M_S cutoff

- $i_D = 0 \Rightarrow v_O = V_H = V_{DD}$
- V_H is set by power supply voltage V_{DD}.
- V_L should be less than V_{TN}, typically $V_L \sim 0.2$ V